

Contents

1	Introduction	1
1.1	Electronics Technologies	2
1.1.1	Printed Circuit Board Technology	2
1.1.2	Hybrid Technology	5
1.1.3	Semiconductor Technology	7
1.2	Integrated Circuits	13
1.2.1	Importance and Characteristics	13
1.2.2	Analog, Digital and Mixed-Signal Circuits	14
1.2.3	Moore’s Law and Design Gaps	17
1.3	Physical Design	21
1.3.1	Main Design Steps	21
1.3.2	Physical Design of Integrated Circuits	23
1.3.3	Physical Design of Printed Circuit Boards	26
1.4	Motivation and Structure of This Book	27
	References	29
2	Technology Know-How: From Silicon to Devices	31
2.1	Fundamentals of IC Fabrication	32
2.2	Base Material Silicon	33
2.3	Photolithography	34
2.3.1	Fundamentals	34
2.3.2	Photoresist	35
2.3.3	Photomasks and Exposure	36
2.3.4	Alignment and Alignment Marks	38
2.3.5	Reference to Physical Design	39
2.4	Imaging Errors	40
2.4.1	Overlay Errors	40
2.4.2	Edge Shifts	42
2.4.3	Diffraction Effects	42
2.4.4	Reference to Physical Design	44

2.5	Applying and Structuring Oxide Layers	45
2.5.1	Thermal Oxidation	46
2.5.2	Oxidation by Deposition	47
2.5.3	Oxide Structuring by Etching	47
2.5.4	Local Oxidation	49
2.5.5	Reference to Physical Design	51
2.6	Doping	52
2.6.1	Background	52
2.6.2	Diffusion	52
2.6.3	Ion Implantation	54
2.6.4	Reference to Physical Design	56
2.7	Growing and Structuring Silicon Layers	58
2.7.1	Homoepitaxy	58
2.7.2	Heteroepitaxy and Polysilicon	61
2.7.3	Reference to Physical Design	62
2.8	Metallization	62
2.8.1	Fundamentals	62
2.8.2	Metallization Structures Without Planarization	65
2.8.3	Metallization Structures with Planarization	67
2.8.4	Reference to Physical Design	71
2.9	CMOS Standard Process	73
2.9.1	Fundamentals: The Field-Effect Transistor	73
2.9.2	Process Options	76
2.9.3	FEOL: Creating Devices	78
2.9.4	BEOL: Connecting Devices	82
	References	82
3	Bridges to Technology: Interfaces, Design Rules, and Libraries	83
3.1	Circuit Data: Schematics and Netlists	84
3.1.1	Structural Description of a Circuit	84
3.1.2	Idealizations in Circuit Descriptions	86
3.1.3	Circuit Representation: Netlist and Schematic	87
3.2	Layout Data: Layers and Polygons	91
3.2.1	Structure of Layout Data	91
3.2.2	How to Read a Layout View	95
3.2.3	Graphics Operations	97
3.3	Mask Data: Layout Post Processing	102
3.3.1	Overview	102
3.3.2	Chip Finishing	102
3.3.3	Reticle Layout	105
3.3.4	Layout-to-Mask Preparation	107

3.4	Geometrical Design Rules	111
3.4.1	Technological Constraints and Geometrical Design Rules	111
3.4.2	Basic Geometrical Design Rules	111
3.4.3	Programmed Geometrical Design Rules	115
3.4.4	Rules for Die Assembly	116
3.5	Libraries	119
3.5.1	Process Design Kits and Primitive Device Libraries	119
3.5.2	Cell Libraries	121
3.5.3	Libraries for Printed Circuit Board Design	123
	References	125
4	Methodologies for Physical Design: Models, Styles, Tasks, and Flows	127
4.1	Design Flow	127
4.2	Design Models	133
4.2.1	Three-Dimensional Design Space	134
4.2.2	The Gajski-Kuhn Y-Chart	136
4.3	Design Styles	139
4.3.1	Full-Custom and Semi-Custom Design	139
4.3.2	Top-Down, Bottom-Up and Meet-in-the-Middle Design	144
4.4	Design Tasks and Tools	146
4.4.1	Creating: Synthesis	146
4.4.2	Checking: Analysis	147
4.4.3	Eliminating Deficiencies: Optimization	148
4.5	Physical Design Optimization and Constraints	148
4.5.1	Optimization Goals	148
4.5.2	Constraint Categories	149
4.5.3	Physical Design Optimization	150
4.6	Analog and Digital Design Flows	151
4.6.1	The Different Worlds of Analog and Digital Design	151
4.6.2	Analog Design Flow	155
4.6.3	Digital Design Flow	157
4.6.4	Mixed-Signal Design Flow	158
4.7	Visions for Analog Design Automation	160
4.7.1	A “Continuous” Layout Design Flow	160
4.7.2	A “Bottom-Up Meets Top-Down” Layout Design Flow	162
	References	164

5 Steps in Physical Design: From Netlist Generation to Layout Post Processing	165
5.1 Generating a Netlist Using Hardware Description Languages	165
5.1.1 Overview and History	165
5.1.2 Elements and Example	167
5.1.3 Flow	168
5.2 Generating a Netlist Using Symbolic Design Entry	169
5.2.1 Overview	169
5.2.2 Elements and Examples	170
5.2.3 Netlist Generation	173
5.3 Primary Steps in Physical Design	174
5.3.1 Partitioning and Floorplanning	175
5.3.2 Placement	180
5.3.3 Routing	183
5.3.4 Physical Design Using Symbolic Compaction	187
5.3.5 Physical Design Using Standard Cells	187
5.3.6 Physical Design of Printed Circuit Boards	189
5.4 Verification	194
5.4.1 Fundamentals	195
5.4.2 Formal Verification	198
5.4.3 Functional Verification: Simulation	199
5.4.4 Timing Verification	200
5.4.5 Geometric Verification: DRC, ERC	202
5.4.6 Extraction and LVS	205
5.5 Layout Post Processing	208
References	210
6 Special Layout Techniques for Analog IC Design	213
6.1 Sheet Resistance: Calculating with Squares	213
6.2 Wells	216
6.2.1 Implementation	216
6.2.2 Breakdown Voltage	218
6.2.3 Voltage-Dependent Spacing Rules	219
6.3 Devices: Layout, Connection, and Sizing	220
6.3.1 Field-Effect Transistors (MOS-FETs)	220
6.3.2 Resistors	224
6.3.3 Capacitors	227
6.3.4 Bipolar Transistors	230
6.4 Cell Generator: From Parameters to Layout	233
6.4.1 Overview	233
6.4.2 Example	234

6.5	The Importance of Symmetry	236
6.5.1	Absolute and Relative Accuracy: The Big Difference	236
6.5.2	Obtaining Symmetry by Matching Devices	237
6.6	Layout Matching Concepts	239
6.6.1	Matching Concepts for Internal Device Fringe Effects	240
6.6.2	Matching Concepts for Unknown Gradients	247
6.6.3	Matching Concepts for External Device Fringe Effects	249
6.6.4	Matching Concepts for Known Gradients	250
6.6.5	Matching Concepts for Orientation-Dependent Effects	252
6.6.6	Summary of Matching Concepts	254
	References	255
7	Addressing Reliability in Physical Design	257
7.1	Parasitic Effects in Silicon	257
7.1.1	Substrate Debiasing	258
7.1.2	Injection of Minority Carriers	261
7.1.3	Latchup	264
7.1.4	Breakdown Voltage, aka Blocking Capability, of p–n Junctions	266
7.2	Surface Effects	267
7.2.1	Parasitic Channel Effects	267
7.2.2	Hot Carrier Injection	270
7.3	Interconnect Parasitics	272
7.3.1	Line Losses	272
7.3.2	Signal Distortions	273
7.3.3	Crosstalk	275
7.4	Overvoltage Protection	275
7.4.1	Electrostatic Discharge (ESD)	276
7.4.2	Antenna Effect	286
7.5	Migration Effects in Metal	290
7.5.1	Electromigration	291
7.5.2	Thermal Migration	292
7.5.3	Stress Migration	293
7.5.4	Mitigating Electromigration	296
7.5.5	Mitigating Thermal and Stress Migration	299
	References	301
	Index	303

Fundamentals of Layout Design for Electronic Circuits

Lienig, J.; Scheible, J.

2020, XV, 306 p. 220 illus., 215 illus. in color.,

Hardcover

ISBN: 978-3-030-39283-3